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**PATENT** 

Case Docket No. ASA-1062

E application of

of T. SASAKI et al

Group Art Unit:

2825

Serial No.:

10/073,312

Filed: February 13, 2002

Examiner:

M. Dimyan

For: DESIGN METHOD AND SYSTEM FOR SEMICONDUCTOR INTEGRATED CIRCUITS

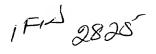
Assistant Commissioner for Patents Washington, D.C. 20231																
Sir:																
Transmitted herewith is an Amendment in the above-identfied application.																
		nall entity status of this application under 37 CFR 1.9 and 1.27 has been established by a verified stement previously submitted.														
	A veri	verified statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.														
X	No additional fee is required.															
The fee has been calculated as shown below:																
	(COL. 1) (COL. 2) (COL. 3)									SMAI	L ENTITY		OTHER THAN A SMALL ENTITY			
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First Presentation of Multiple Dependent Claims									+	140	\$	1	+	280	\$	
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** If the entry in Col. 1 is less than the entry in Col. 2, write U'in Col. 3.  ** If the 'Highest Number Previously Paid For' IN THIS SPACE is less than 20, write '20' in this space.  ** If the 'Highest Number Previously Paid For' IN THIS SPACE is less than 3, write '3' in this space.  The 'Highest Number Previously Paid For' (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior Amendment or the number of claims originally filed.																
	Please charge my Deposit Account No. 50-1417 in the amount of \$															
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Date: June 30, 2004

В

Daniel J. Stanger Registration No. 32,846 Attorney for Applicant(s)





ASA-1062

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. SASAKI et al

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SEMICONDUCTOR INTEGRATED CIRCUITS

## REPLY

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In reply to the Office Action mailed March 30, 2004, please amend the above-identified application as follows. A certified copy of Japanese priority Patent Application No. 2001-038678 accompanies this Reply in satisfaction of the requirement set forth in 35 U.S.C. §119.

## IN THE TITLE

Please amend the title of the invention to --DESIGN
METHOD AND SYSTEM FOR ACHIEVING A MINIMUM MACHINE CYCLE FOR
SEMICONDUCTOR INTEGRATED CIRCUITS--.